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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,664	08/25/2003	Tony Mai	2037.2038-001(11067-01US-	2135

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/647,664	MAI, TONY	
	Examiner	Art Unit	
	Emmanuel Bayard	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 5/31/07 in which claims 1-15 are pending. The amendment has been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-xxx are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al U.S. Pub No 2007/0007941 A1.

As per claim 1, Lin et al teaches a delay locked loop (see fig. 2 element 32) comprising: a delay circuit which provides a delay (see fig.2 element 42) to a reference clock (see fig.2 element 34) to generate a feedback clock (see fig.2 element feedback), the delay circuit having a delay range (see page 1 [0007]); a phase detector which compares phase of the reference clock and the feedback clock to change the delay of the delay circuit (see fig.2 element 46); and an initialization circuit that after reset of the delay locked loop (see page 3 [0030]) assures that the phase detector initially changes the delay in a direction away from a first end of the delay range after receipt of one of the reference clock and feedback clock and enables a change in the delay in an

opposite direction toward the first end only after receipt of one of the reference clock and feedback clock followed by receipt of the other of the reference clock and feedback clock (see abstract and page 1 [0011]).

As per claim 2, Lin et al teaches 1 wherein the first end of the delay range is a minimum delay and the direction away from the first end increases the delay and the opposite direction towards the first end decreases the delay (see paragraphs [0006], [0033-0034]).

As per claim 3, Lin et al teaches wherein the initialization circuit increases the delay after receipt of the reference clock and enables decrease in the delay only after receipt of the reference clock followed by the feedback clock (see paragraphs [0006], [0033-0034]).

As per claim 6, Lin et al inherently teaches wherein the first edge of the reference clock is a rising edge and the edge of the feedback clock is a rising edge (see paragraphs [0006]).

As per claims 9 and 13, Lin et al teaches method for initializing a delay locked loop comprising the steps of: providing a delay (see fig.2 element 42) to a reference clock (see fig.2 element 34) to generate a feedback clock (see fig.2 element Feedback), the delay circuit being initially set at a first end of a delay range; comparing phase of the reference clock and the feedback clock to change the delay of the delay circuit (see fig.2 element 46) and page 1 [0007]); after reset of the delay locked loop assuring that the delay initially be changed in a direction (see page 3 [0030]) away from the first end of the delay range after receipt of the reference clock; and enabling a change in the

delay in an opposite direction toward the first end only after receipt of the reference clock followed by receipt of the feedback clock (see abstract and page 1 [0011]).

As per claim 10, Lin et al teaches wherein the first end of the delay range is a minimum delay and the direction away from the first end increases the delay (see paragraphs [0006], [0033-0034]).

As per claim 11, Lin et al inherently teaches further comprising the steps of: delaying enabling adjustment of the delay (see abstract) in the first direction until a first predetermined number of the reference clock edges are detected; and delaying enabling adjustment (see fig.2 element 8d) in the opposite direction until a second predetermined number of the reference clock edges are detected (see paragraphs [0006], [0009] [0033-0034]).

As per claim 12, Lin et al inherently teaches wherein the first edge of the reference clock is a rising edge and the edge of the feedback clock is a rising edge. Note since both the reference clock and the feedback clock are being compared in the phase comparator, edge detection is inherently performed to determine the rising and falling transition in both clocks.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4-5, 7-8 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al U.S. Pub No 2007/0007941 A1 in view of Yoshimura et al U.S. Patent N0 5,994,934.

As per claims 4 and 7, Lin et al teaches all the features of the claimed invention wherein the initialization circuit enables change in the delay in the direction away from the first end and to enable change in the delay in the opposite direction except an initialization circuit comprises a first latch responsive to the reference clock which detects a first edge of the reference clock and a second latch responsive to the feedback clock which detects an edge of the feedback clock after the first edge of the reference clock has been detected by the first latch, the input of the second latch coupled to the output of the first latch.

Yoshimura teaches an initialization circuit comprises a first latch responsive to the reference clock which detects a first edge of the reference clock (see fig.10 element 52) and a second latch responsive (see fig.10 element 57) to the feedback clock which detects an edge of the feedback clock (see fig.10 element FBCLK) after the first edge of the reference clock has been detected by the first latch, the input of the second latch coupled to the output of the first latch.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Yoshimura et al into Line et al so that the internal reset signal could retain "H" during two cycles periods of the feedback signal, causing no influence as taught by Yoshimura et al (see col.15, lines 35-40).

As per claim 5, Yoshimura teaches wherein the initialization circuit further

comprises: a third latch (see fig.10 element 53) and a fourth latch (see fig.10 element 58). Furthermore combining the teaching of Yoshimura and Lin et al to perform: a third latch responsive to the reference clock which detects a next edge of the reference clock to delay enabling change in the delay in the first direction for at least one reference clock period, the input of the third latch coupled to the output of the first latch; and a fourth latch responsive to the feedback clock which detects a next edge of the feedback clock to delay the enabling of change in the delay in the opposite direction for at least one feedback clock period, the input of the fourth latch coupled to the output of the third latch would have been obvious to one skilled in the art as to detect an erroneous state and recover to a normal state quickly. Furthermore implementing such teaching into Lin et al would have been obvious to one skilled in the art so that the internal reset signal could retain "H" during two cycles periods of the feedback signal, causing no influence as taught by Yoshimura et al (see col.15, lines 35-40).

As per claim 8, Yoshimura teaches wherein the phase detector comprises: a latch responsive to the reference clock to generate a first phase control signal (see fig.2 element 4U); and another latch responsive to the feedback clock to generate a second phase control signal (see fig.2 element 4D). Furthermore implementing such teaching into Lin et al would have been obvious to one skilled in the art as to detect an erroneous state and recover to a normal state quickly.

As per claim 14, Lin et al teaches all the features of the claimed invention wherein the initialization circuit enables change in the delay in the direction away from the first end and to enable change in the delay in the opposite direction except an

initialization circuit comprises a first latch responsive to the reference clock which detects a first edge of the reference clock and a second latch responsive to the feedback clock which detects an edge of the feedback clock after the first edge of the reference clock has been detected by the first latch, the input of the second latch coupled to the output of the first latch.

Yoshimura teaches an initialization circuit comprises a first latch responsive to the reference clock which detects a first edge of the reference clock (see fig.10 element 52) and a second latch responsive (see fig.10 element 57) to the feedback clock which detects an edge of the feedback clock (see fig.10 element FBCLK) after the first edge of the reference clock has been detected by the first latch, the input of the second latch coupled to the output of the first latch.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Yoshimura et al into Line et al so that the internal reset signal could retain "H" during two cycles periods of the feedback signal, causing no influence as taught by Yoshimura et al (see col.15, lines 35-40).

As per claim 15, Yoshimura and Lin et al in combination would teach, wherein the initialization circuit enables the first latch after receipt of a first plurality of said one of the first and second input signals and enables the second latch only after enabling the first latch and the receipt of a second plurality of said other of the first and second input signals as to detect an erroneous state and recover to a normal state quickly.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571 272 3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

8/13/2007

Emmanuel Bayard
Primary Examiner
Art Unit 2611

EMMANUEL BAYARD
PRIMARY EXAMINER